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US Army Research Laboratory

Ka Band Channelized Receiver

by John T Clark, Andre K Witcher, and Eric D Adler

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14. ABSTRACT

The design of a 30-channel Ka band receiver is described in detail including both the radio frequency (RF) down-conversion architecture and the digital signal processing platform to be used. The system, which is composed entirely of commercial-off-the-shelf (COTS) components, is capable of covering 44% of the entire Ka band including the Future Combat Systems Radar and Communications Band in real time with the capability of determining the input signal spectrum location.

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1. Introduction

For electronic warfare (EW) requirements covering the Ka band spectrum, a channelized receiver is highly desirable. Additionally the Future Combat Systems (FCS) Radar and Communications allocations reside in this band of the spectrum. This report defines a first-order system analysis of constructing an analog radio frequency (RF) channelized receiver that converts the spectrum from 34 to 40 GHz into thirty 200-MHz channels. The RF design caters to the state of the art in digital signal processing hardware and software algorithms. RF commercial-off-the-shelf (COTS) parts are selected in order to develop a system baseline for size, weight, power, and cost requirements (SWaP-C). Data acquisition of the selected Ka band span is accomplished by translating each 200-MHz channel down to a common intermediate frequency (IF) and sampling with a multi-channel reconfigurable oscilloscope from a National Instruments (NI) PXI platform.

2. Approach

The NI digitizer PXIe-5171R is a 14-bit, 8-channel reconfigurable oscilloscope with 300 MHz of analog bandwidth per channel. This signal processing architecture is capable of sampling eight 200-MHz channels simultaneously. Four of these cards allow a design that covers the full spectrum where the sampling occurs at a common IF from 100–300 MHz in all 30 channels. The processing algorithm, channel, and card position within the PXIe chassis determines the detected input frequency. Table 1 provides a correlation index between the detection input frequency and an applied frequency offset generated with a coherent array of external phase locked dielectric resonator oscillators (EPLDROs).

Table 1 Scope correlation index for the detection input frequency

Card	Channel	Offset (GHz)	Input Frequency (GHz)
1	1	33.9	34.0–34.2
1	2	34.1	34.2–34.4
1	3	34.3	34.4–34.6
1	4	34.5	34.6–34.8
1	5	34.7	34.8–35.0
1	6	34.9	35.0–35.2
1	7	35.1	35.2–35.4
1	8	35.3	35.4–35.6
2	1	35.5	35.6–35.8
2	2	35.7	35.8–36.0
2	3	35.9	36.0–36.2
2	4	36.1	36.2–36.4
2	5	36.2	36.4–36.6
2	6	36.3	36.6–36.8
2	7	36.5	36.8–37.0
2	8	36.7	37.0–37.2
3	1	36.9	37.2–37.4
3	2	37.1	37.4–37.6
3	3	37.3	37.6–37.8
3	4	37.5	37.8–38.0
3	5	37.7	38.0–38.2
3	6	37.9	38.2–38.4
3	7	38.1	38.4–38.6
3	8	38.3	38.6–38.8
4	1	38.5	38.8–39.0
4	2	38.7	39.0–39.2
4	3	38.9	39.2–39.4
4	4	39.1	39.4–39.6
4	5	39.3	39.6–39.8
4	6	39.5	39.8–40.0

3. RF Design and RF Parts

The total spectrum bandwidth from 34 to 40 GHz is received with a COTS antenna and low-noise amplifier (LNA), followed by down-conversion to a 2–8 GHz IF, where the channelization takes place through COTS power dividers. The LNA has sufficient gain that the overall receiver noise figure is not degraded by subsequent components and its noise figure, when added to the thermal noise, is the minimum detectable signal. Each channel is further down-converted into a common IF

(100–300 MHz) through the coherent array of ERDROs. Figure 1 illustrates the RF components needed to perform this action. These components are detailed below. All filtering is performed digitally. Table 2 lists the total RF parts cost, size, and power requirements. It is expected that all RF hardware, including power supplies, can be integrated into a 19-inch rack that is 24 inches deep and 4 inches high.

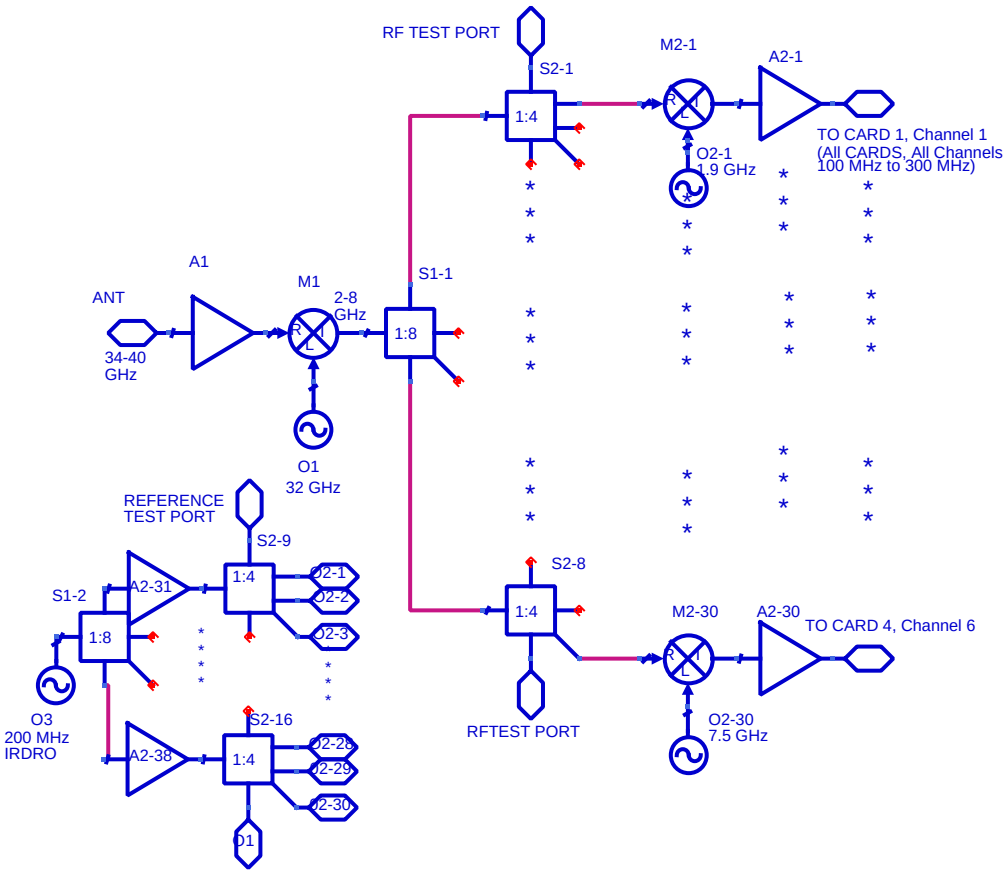

Fig. 1 RF schematic (note the reference distribution network is shown in lower left corner)

Table 2 Parts list for the RF components

Part	Make	Model	Qty	Unit Cost	Total Cost	Size (L X W X H) in	Vdc (V)	Idc(A)	Pdc(W)
ANT	Quinstar	QWH-Ka	1	$1,450.00	$1,450.00	4.2 X 1.87 X1.87	0	0	0
A1	Miteq	JS44-18004000-33-8P	1	$2,850.00	$2,850.00	0.74X 0.93 X 0.35	15	0.4	6
O1	Lucix	ERDRO (32 GHz)	1	$2,175.00	$2,175.00	2 X 1.883 X 0.652	15	0.2	3
M1	Miteq	TB0440LW1	1	$795.00	$795.00	0.52 X 0.56 X0.29	0	0	0
S1	MCL	ZN8PD-113+	2	$300.00	$600.00	6.6 X 3.28 X 0.75	0	0	0
S2	Crane	PDM-44M-10G	16	$525.00	$8,400.00	2 X 2 X 0.38	0	0	0
O2	Lucix	ERDRO (1.9:0.2:7.5)	30	$795.00	$23,850.00	2 X 1.883 X 0.652	15	0.325	146.25
M2	MCL	ZX05-ED12902/7	30	$350.00	$10,500.00	0.75 X 0.9 X 0.54	0	0	0
A2	MCL	ZKL-2+	38	$139.95	$5,318.10	1.5 X 1.38 X 0.5	12	0.12	54.72
O3	Lucix	IRDRO (200 MHz)	1	$1,350.00	$1,350.00	2 X 1.883 X 1.28	12	0.67	8.04
TOTAL			120		$57,288.10				218.01
V and I are per unit quantities, Power is for Qty*Unit (V*I)									

Note: MCL=Mini-Circuits, Crane is the owner of the formerly Merrimac products; L3 Communications is the owner of the formerly MITEQ products.

3.1 Ka Antenna

Quinstar's QWH-Ka model covers 26.5 to 40 GHz with a max voltage standing wave ratio (VSWR) of 1:10:1 and a gain of 21 dB in a conical form factor (24 dB in a pyramidal form factor). The conical version is shown in Fig. 2.

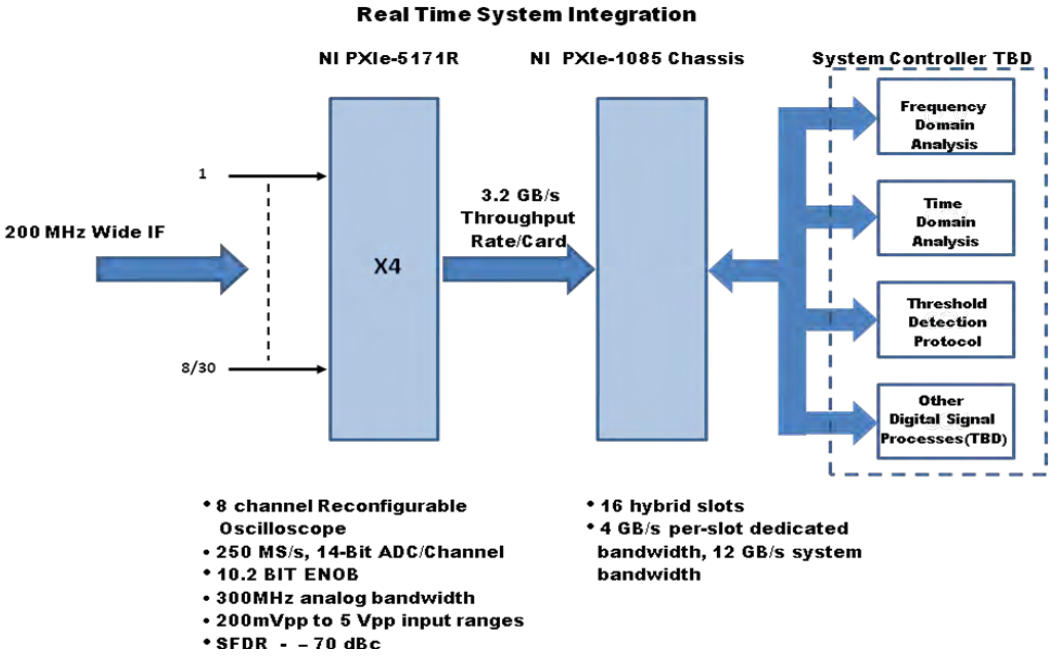

Fig. 2 Real-time system processes and integration plan

3.2 Ka LNA

MITEQ's JS44-18004000-33-8P has at least 48 dB of gain from 18 to 40 GHz a maximum noise figure of 3.3 dB and an output 1-dB compression point (1dBCO) of +8 dBm. It consumes 6 W of DC power. The compression power referred to the input requires input signals to be no greater than –40 dBm.

3.3 Ka Mixer

MITEQ's TB044LW1 triple balanced mixer can mix RF input signals from 34 to 40 GHz with a local oscillator (LO) to produce IF outputs anywhere between 500 MHz to 20 GHz. The conversion loss is at most 13 dB (the overall gain is now 35 dB). Using a single ERDRO at 32 GHz, the input range of 34 to 40 GHz is down-converted to 2 to 8 GHz and then presented for channelization.

3.4 Power Divider

Thirty channels are created by dividing the input 32 ways, which provides 2 extra ports that can be used as test ports or terminated (channels 7 and 8 on card 4). To avoid custom parts, the 32-way division is accomplished with 1 COTS 8-way divider followed by 8 COTS 4-way dividers: Mini Circuit's ZN8PD-113+ and Crane's PDM-44M-10G, respectively. They have insertion losses of 11.9 and 8 dB, respectively (the overall gain is now 15.1dB).

3.5 Baseband Mixer

There are 30 instances of this mixer: Mini-Circuits ZX05-ED12902/7, which has a typical conversion loss of 6 dB (the overall gain is now 9.1 dB). These mixers are mated with a series of offset ERDROs that mix all inputs down to 100 to 300 MHz. The first ERDRO is at 1.9 GHz, the next steps by 200 MHz to 2.1 GHz, and so on until the last one, which is at 7.5 GHz. The frequency offset, shown in Table 1, is the sum of the first 32-GHz ERDRO and the second ERDRO used at the baseband mixer (i.e., for card 1, channel 1, 32 GHz+1.9 GHz=33.9 GHz). For the test ports, there is no baseband mixing, so the frequency offset is simply 32 GHz.

3.6 Baseband Amplifier

There are 30 instances of this amplifier, a Mini-Circuits ZKL-2+, which has a minimum gain of 31 dB, a 1dBCO of +16.4 dB, and a noise figure of 3.5 dB. This is the last component in the receiver before presentation to the PXI card channels. At this point, the overall gain is 40.1 dB, the overall noise figure is 3.83 dB, and the receiver compresses for all input signals above –40 dBm. This maximum input signal is amplified to approximately 0 dBm at the signal processor input. The signal processor has an effective number of bits of at least 10.2, so a dynamic range of at least 61 dB is achievable.

3.7 Local Oscillators

Lucix's EPLDROs provide the best phase noise performance and accuracy available to drive the mixers. All units lock to a 200-MHz reference that is provided by an internal reference DRO (IRDRO). The IRDRO determines the phase noise of the EPLDRO. The IRDRO has the following phase noise characteristics:

- at a 100-Hz offset = –94 dBc/Hz,
- at a 1-kHz offset = –119 dBm/Hz,
- at a 10-kHz offset = –129 dBm/Hz,

- at a 100-kHz offset = –140 dBc/Hz, and
- at a 1-MHz offset = –144 dBc/Hz.

This reference uses another 8-way divider followed by 8 baseband amplifiers and then 8 more 4-way dividers to distribute the reference at an appropriate level to all 31 ERDROs. The remaining port is a test port to verify the presence and strength of the reference. There is one 32-GHz ERDRO and 30 ERDROs ranging from at 1.9 to 7.5 GHz in 200-MHz steps. See Table 2 for a parts list for the RF design.

4. Signal Processing Design

Figure 2 depicts the system process flow from the 100 to 300 MHz, baseband IF through an 8-channel x 4 digitizer cards, for a total of 30 dedicated channels, each with a bandwidth of 200 MHz. Each channel converts the incoming signal to 14-bit digital words for further system processing. Those processes consist of frequency, time-domain analysis, threshold and level detection protocols, or other user-defined processes.

4.1 National Instruments (NI) Digitizer

The PXIe-5171R, shown in Fig. 3, is a 14-bit, 8-channel reconfigurable oscilloscope with 300 MHz of analog bandwidth per channel. A reconfigurable oscilloscope means that the scope's embedded software can be replaced by a custom real-time instrument design for customized real-time signal analysis running on a field-programmable gate array (FPGA). This gives the user the flexibility of performing system and signal processing tasks deterministically, which minimizes the dead time and overhead constraints usually associated with a modern central processing unit (CPU) or embedded software. Four digitizer cards are needed to meet the 30-channel requirements. The digitizer samples signals at a rate of 250 MS/s per channel simultaneously. The spurious free dynamic range (SFDR) is specified at –70 dBc. The digitizer effective number of bits (ENOBs) is specified at 10.2 bits. From the ENOB specification, the signal-to-noise ratio (SNR) for the digitizer can be calculated as 6 dB per bit for a 61-dB SNR.

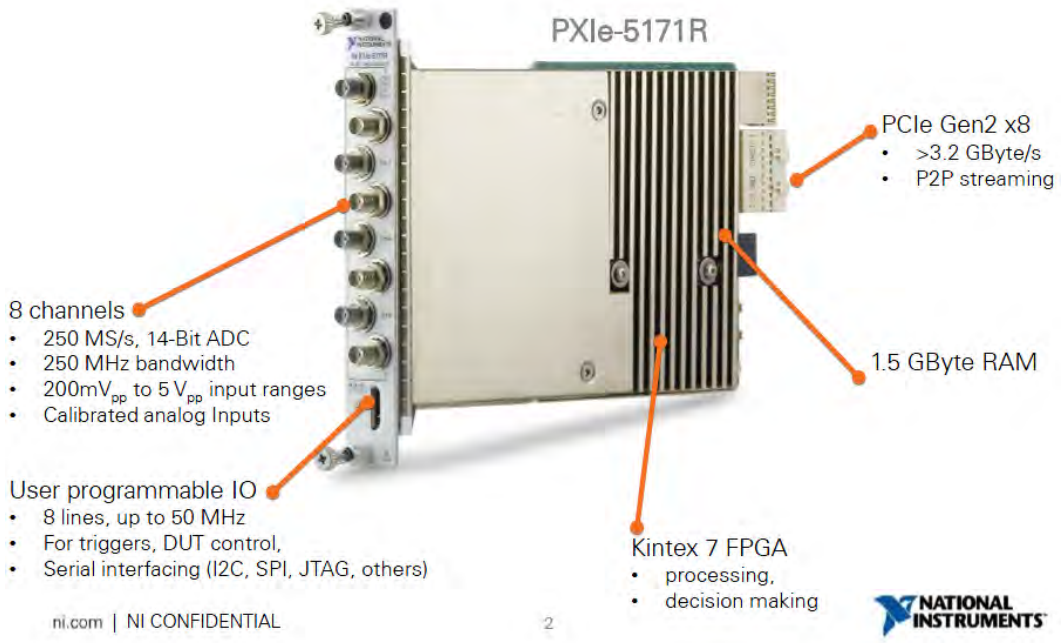

Fig. 3 PXIe-5171R 8-channel reconfigurable oscilloscope (reproduced with permission)

The 5171R has a 3.2-GB/s throughput rate when installed in a NI PXIe-1085 chassis, depicted in Fig. 4. The 1085 is an 18-slot chassis with 16 hybrid slots, which mean that other modules outside of the NI product family can be incorporated to take advantage of their capability to expand the overall user capability of the system. Two slots are reserved for the system controller to be determined (TBD). The overall system bandwidth of the chassis is 12 GB/s.

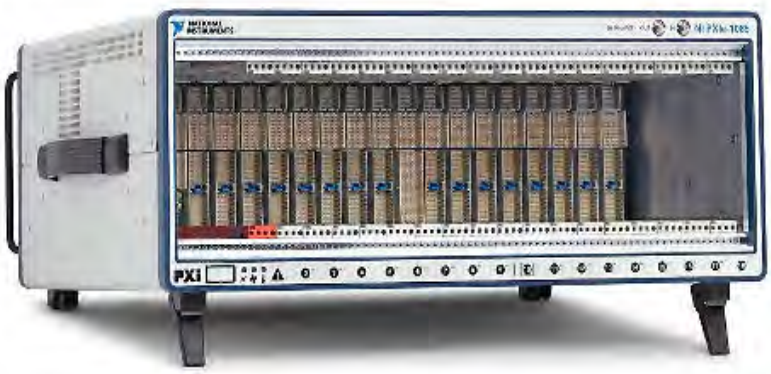

Fig. 4 PXIe-1085 18 slot chassis (reproduced with permission)

Once the incoming baseband signal is detected and processed, further analysis can be performed in determining, for example, the frequency of the detected signal by measuring the offset of signal and adding it to the frequency of the LO for that channel. If, for example, a signal is present in card 3, channel 1 of the system at

210 MHz, the offset frequency (determined by a lookup-word derived from Table 1) of 36.9 GHz would be added to 210 MHz yielding 37.11 GHz as the received input signal frequency. Other system parameters can be measured and functions performed depending on user requirements.

4.2 Digital Filtering

To further mitigate the components of SWaP-C, it is proposed that all filtering be performed in software after down-conversion to baseband. Through the use of in-band finite impulse response (FIR) filter banks, as depicted in Fig. 5 as FL1 to FL30, the signal appearing in that pre-configured and dedicated band would be processed to determine, for example, the center frequency of that signal and also any other parameter defined by the user. Each filter would be band passed to tightly filter 100 to 300 MHz while excluding all other frequencies. Adjacent channels would mix into the DC 100 or 300 MHz and above range, thus the channel selectivity would be accomplished at this point via the FIR filters. This would also serve to mitigate false alarms. Each of these bands could be further subdivided for further signal identification and classification queries. The signal processing cost estimates are provided in Table 3.

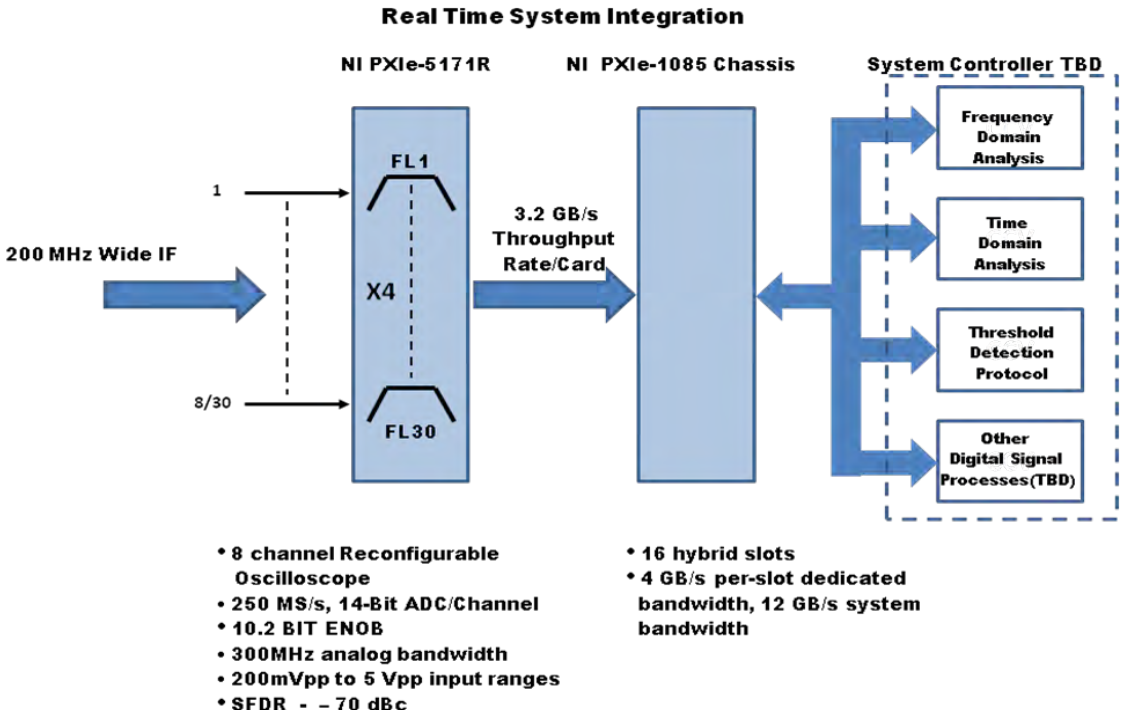

Fig. 5 Real-time system process and integration plan incorporating FIR filter banks

Table 3 Signal processing cost estimates

Manufacturer	Type	Part No.	Qty	Cost	Total
NI	ADC/Digitizer	PXIe-5171R	4	11,999.00	$47,996.00
NI	Chassis	PXIe-1085	1	8,999.00	$8,999.00
NI	System Controller	PXIe-8135	1	6,149.00	$6,149.00
					$63,144.00

Note: Software TBD.

5. Conclusion

A market analysis and design study was conducted to determine the feasibility of implementing an EW requirement for a Ka band channelized receiver with a spectrum coverage from 34 to 40 GHz in thirty 200-MHz-wide bands. The market analysis revealed that a COTS implementation to meet the requirement would be a most practical and cost-effective solution. The estimated hardware cost of the baseline design, which includes the RF framework and digital signal processing unit, would be approximately $125K.

The complete size and weight would be dependent on the integration, power requirements, final assembly, and packaging of the complete system. The system would consume approximately 1.5 kW of AC power. Higher levels of RF integration could be achieved to shrink the system, yet it would involve a non-recurring engineering (NRE) investment. The cascade analog RF analysis yields a maximum signal of –40 dBm and a thermal noise floor of –91 dBm (with a 200-MHz final IF). Adding a system noise figure of 3.5 dB raises that floor to –87.5 dBm. Thus, the analog dynamic range is 47.5 dB across the selected 6 GHz of the Ka band. However, the digital signal processing has a dynamic range of 61 dB, thus approximately 13.5 dB of processing gain is expected from the channelized receiver.

List of Symbols, Abbreviations, and Acronyms

1dBCO	Output 1-dB compression point
COTS	commercial-off-the-shelf
CPU	central processing unit
ENOBs	effective number of bits
EPLDROs	external phase locked dielectric resonator oscillators
EW	electronic warfare
FIR	finite impulse response
IF	intermediate frequency
IRDRO	internal reference Dielectric Resonator Oscillator
LNA	low-noise amplifier
LO	local oscillator
NI	National Instruments
NRE	non-recurring engineering
RF	radio frequency
SFDR	spurious free dynamic range
SNR	signal-to-noise ratio
SWaP-C	size, weight, power, and cost
TBD	to be determined
VSWR	voltage standing wave ratio

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